## IN THE UNITED STATES PATENT OFFICE

In Re Patent of

Application No. 10/002,713

First Named Inventor: Ichiriu, Michael E.

Confirmation No. 3008

Patent No.: 7,043,673

Issue Date: 5/9/2006

For: Content Addressable Memory with

PRIORITY-BIASED ERROR DETECTION

SEQUENCING

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

## Statement Under 37 CFR §3.73(b)

Sir:

NetLogic Microsystems, Inc., a Delaware corporation, hereby states that it is the assignee of the entire right, title and interest in the above-identified patent by virtue of the Assignments that are recorded in the USPTO at Reel/Frame 012351/0078.

The undersigned is authorized to act on behalf of the assignee at least for purposes of making the foregoing statement.

Effective immediately, please direct all further communications in the aboveidentified patent application to the following address:

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Respectfully submitted,
MAHAMEDI PARADICE KREISMAN LLP

Date \_\_\_\_\_February 10, 2010

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